BITSILICA PVT. LTD.

&

P. Chandrasekhar, Professor, Dept. ECE, OUCE, Osmania University

&

Chaitanya Bharathi Institute of Technology (A), Hyderabad

Memorandum of Understanding

For the execution of the following project

Project:	The design, fabrication and development of silicon proven IP Core for high resolution ADPLL
Funding Agency:	Ministry of Electronics & Information technology (MEITY), Govt. of India
Under the Scheme:	Chip to Startup (C2S) Scheme

This memorandum of understanding ("MOU") is executed on this day 07-10-2022

The "MoU" is signed solely for the purpose of execution of the Project-A prosed to MEITY under C2SD Scheme. The title of the Project-A is "**The design, fabrication and development of silicon proven IP Core for high resolution ADPLL**". Hereinafter called Project-A-A.

The MOU signed is conditional. All the terms below will take effect solely based on MEITY accepting the proposed **Project-A-A** for funding. In case the MEITY rejects the proposed Project-A-A, this MoU will be treated as NULL and VOID.

BITSILICA Pvt. Ltd represented by **Mr. Rajasekharam Naidu P.** Director of Embedded Solutions. It is having its registered office at 3rd Floor, Dwaraka Heights, Plot No. 17, Jubilee Enclave, Madhapur, Hyderabad, Telangana 500081. Hereinafter called Party I:

Prof. P. Chandra Sekhar, Department of ECE, Osmania University, Hyderabad, 500 007 Hereinafter called Party II:

Chaitanya Bharathi Institute of Technology(A), Hyderabad, 500 075. Hereinafter called Party III:

Prof. P. Chandra Sekhar
Dept of Electronics and Communication Engineering
Osmania University, Hyderabad-500 007.

ARTICLE-1: Scope of the MoU

The scope of this MOU signed among OUCE(A), BITSILICA Pvt. Ltd. and CBIT(A) is restricted only during/ for the period of execution of the Project-A. The details of Project-A are as follows.

Project-A: **The design, fabrication and development of silicon proven IP Core for high resolution ADPLL**

Agency: **MEITY, GoI**

Scheme:**C2S Scheme**

This MOU is conditional. i.e., all the terms of this MoU will take effect only after MEITY's acceptance of the proposed **Project-A** for funding. In case the MEITY rejects the proposed Project-A, this MoU and all the terms herein shall be treated as NULL and VOID.

ARTICLE-II : Responsibilities

A. RESPONSIBILITIES OF PARTY-I:

1) To provide commercially driven state of the art technical specification required for the project-A.
2) To provide acceptance specification for the ASIC.
3) To provide necessary technical information, guidance, and support for the successful execution of the project.
4) To attend Project review meetings by nominating a suitable representative along with the representatives of the other parties involved in the execution of Project-A.
5) To release the funds promised for the execution of the project in appropriate time frame as specified in the proposal of project-A based on approved milestones.
6) To provide necessary technical support and industry level training for the staff of the Project-A as required in different stages of the project.
7) To help characterize/test and validate the fabricated ASIC.
8) To obtain necessary certification for the final IP core.
9) To validate the design as per the required specifications.
10) To be responsible for industry level validation for the pre-layout, post-layout and fabricated ASIC.
11) To commercialize the IP according to it's marketing strategy.
12) To enhance the quality of education imparted by Party-II & Party-III by providing necessary support.
13) To suggest for design / revision of course curriculum of the PG Degree / Certificate Programs run by Party-II & Party-III in VLSI Design.

B. RESPONSIBILITIES OF PARTY-II:

1) To be collaborator in the proposed Project-A.
2) It is responsible for design and development of following sub circuits / Circuits specifically as per the required acceptance specifications.
    a. High resolution DCO with less phase noise.
    b. Delta Sigma Modulator - for refining resolution of DCO.
    c. other low noise mechanism - for DCO.
    d. Integration of complete ADPLL for BLE-Low Energy applications.
3) To develop layout, post layout validation of the ADPLL including EMI/EMC validations and Generation of GDS-II.
4) To be single point of contact with MEITY during the entire Project-A duration.
5) To attend all the project review meetings whenever required.
6) To disseminate the information parties received from MEITY related to the Project-A among other parties.
7) To generate appropriate Number of PhD /Post Graduates/Graduates in the field of Embedded Systems/VLSI/Microelectronics/etc. as specified in the Project-A proposal submitted to MEITY.
8) To generate/apply 1(one) Indian patent in the field related to the Project-A.
9) To produce 2 Journal publications of sufficient quality in the field related to the Project-A.
10) To produce 2 Conference presentations in the field related to the Project-A.
11) To review progress of the work of the participating institute.
12) To provide necessary technical support to the participating institute in implementation of the Project-A including procurement of the required software from MEITY and training of the Staff.
13) To share the technical details related to the progress of the Project-A with other parties on timely basis.
14) To maintain the records of all accounts related to the Project-A.
15) To transparently and proportionally disburse the funds received from funding agencies to the participating institute.
16) To distribute the grant received from the funding agency to participating institute for procurement of any hardware/ software required for the completion of the Project-A within the time frame specified in the Project-A proposal.
17) To procure the fabricated ASIC after fabrication by MEITY and sharing of the same with participating Institute for testing/ validation/characterization purpose.
18) To deliver the final GDS-II design to the MEITY accepting all the necessary terms and conditions.
19) To exchange ASIC related information with the industrial partner and participating.

institutes.

C. RESPONSIBILITIES OF PARTY-III:

1) To be collaborator in the proposed Project-A.
2) Responsible for complete schematic level design, verification, layout generation and post layout verification, validation of the following modules/ circuits /sub-modules / sub- circuits
    a. Phase Detector - for ADPLL.
    b. Coarse TDCs - for ADPLL.
    c. Fine TDCs - for ADPLL
    d. Digital Loop Filter - for ADPLL.
3) Communicate and update project status with OUCF (Nodal Center) for smooth execution of the project-A.
4) To immediately inform any serious issues that may affect the execution of the Project-A to the other parties involved
5) To generate appropriate Number of PhD / Post Graduates /Graduates in the field of Embedded Systems/VLSI/Microelectronics/etc. as specified in the Project-A proposal submitted to MEITY.
6) To produce 2 Journal publications of sufficient quality in the field related to the Project-A.
7) To produce 2 Conference presentations in the field related to the Project-A.
8) To present the progress of the work to the nodal centre and resolving subsequent queries related to the Project-A.
9) To provide necessary technical support to other parties necessary in the implementation of the Project-A.
10) To share the technical details related to the progress of the Project-A with other parties on timely basis.
11) To maintain the records of all accounts related to the Project-A received from the Nodal Centre.
12) To Pay the salaries of the manpower involved in the timely basis.
13) To Procure any hardware/ software required for the completion of the Project-A within the time frame specified in the Project-A proposal immediately after receiving the grant from the Nodal Centre.
14) To procure the fabricated ASIC from Nodal Centre for testing/ validation/characterization purpose.
15) To handover the ASIC to the Nodal Centre after completion of the testing/validation/characterization.

D. JOINT RESPONSIBILITIES:

1) The release of any information will be maintained confidential with mutual agreement of both parties.

2) Neither party shall have any liability except what is expressly mentioned herein.

3) While undertaking a joint program the expertise, software, hardware, data, etc., available with either party will be made available for completion of the project.

ARTICLE-III: IPR

1) Rights regarding ownership of the ASIC IP & other IPs developed as part of the Project-A as per the mutually agreed terms and conditions is decided to be in the proportion 20:40:40 for Party-I: Party-II: Party-III

2) If the Party-1 has overseas / global operations / presence, the IP rights belongs to India and the Indian Unit of the Party-I.

ARTICLE-IV: SHARING of FACILITIES

1) Party-1 shall nominate experts in VLSI to deliver industrial level technical training / guidance to the staff /student of Party-II and Party-III when required on mutual agreement.

2) All parties shall provide the access to all the equipment procured as part of the Project-A to the other parties collaborating in the project-A for testing /characterization/validation purposes.

ARTICLE-IV: EFFECTIVE DATEs and DURATION of the MOU

1) This MOU is conditional, it will take effect of Ministry if Electronics and Information Technology (MEITY). Government of India accepts the proposal of Project-A for funding. The MoU will come into effect after it's approval by competent authorities and after MEITY's approval of the Project-A.

2) The duration of the MoU is up to the duration of execution of the Project-A and may be extended or terminated based on mutual agreement with a notice period of three months. However, the termination of MoU may in no manner affect the execution of the project and the staff involved.

ARTICLE-V: AMENDMENTS

Any amendments and/or addenda to the AGREEMENT should be in writing and signed by the parties hereto and shall only after such execution be deemed to form part of the AGREEMENT and have the effect of modifying the AGREEMENT to the extent required by such amendment

CBIT

or addenda.

For:	For:	For:
Chaitanya Bharathi Institute of Technology(A) Hyderabad. (Party-III`)	P. Chandra Sekhar OUCE(A). Hyderabad (Party-II)	BIT SILICA Pvt. Ltd. (Party-I)
By: Dr. P. Ravinder Reddy Principal.	By: Prof. P. Chandra Sekhar Professor. Dept. of ECE. OUCE(A)	By: Rajasekharam Naidu P Director. Embedded Systems

Prof. P. Chandra Sekhar
Dept. of Electronics & Communication Engineering
Osmania University, Hyderabad-500 007.

CHAITANYA BHARATHI CBIT HYDERABAD INSTITUTE OF TECHNOLOGY

BIT SILICA PRIVATE LTD. HYDERABAD

BITSILICA
VLSI Embedded Systems AI

PART IV
LETTER OF INTEREST FROM END USER ORGANIZATION

1. Project Title: *The design, fabrication and development of silicon proven IP Core for high resolution ADPLL*

2. Duration: *5-Years*

3. Name of End User Organization: BITSILICA Pvt. Ltd.

4. Brief Business/Organization Profile: *BITSILICA is supporting clients in developing complex ASICs/SoCs with our expertise in processors, mobile, networking, automotive, 5G and multimedia technologies. We offer a wide range of 'Concept-to-Pre-Silicon' Design services including Design Specification, RTL Design, Functional Verification, Logic Synthesis, Physical Design and STA. At present we offer services to more than 20 clients at various stages of SOC development.*

5. Roles & Responsibility defined under the Project

   a) To provide commercially driven state of the art technical specification required for the project-A.
   b) To provide necessary technical information, guidance, and support for the successful execution of the project.
   c) To attend Project review meetings by nominating a suitable representative along with the representatives of the other parties involved in the execution of Project.
   d) To release the funds promised for the execution of the project in appropriate time frame as specified in the proposal of project based on approved milestones.
   e) To help characterize/test and validate the fabricated ASIC.
   f) To obtain necessary certification for the final IP core.
   g) To be responsible for industry level validation for the pre-layout, post-layout and fabricated ASIC.
   h) To commercialize the developed IPs.in the Project.

- Specifications of the PROPOSED ADPLL IP
  - Electrical Specifications
    - i. VDD= 1- 1.8 Volt
    - ii. Power=2.5mWatt
    - iii. Technology= 45nm TSMC (preferably)
  - Functional Specifications
    - i. Frequency Range: 2.4 - 2.48GHz
    - ii. Frequency Resolution: < 65kHz (<150kHz for BLE)
    - iii. Target Phase Noise Performance

iv. In-Band Phase Noise: < -75dBc/Hz
v. Out of Band Phase Noise: < -100dBc/Hz
vi. Settling Time = 15us
vii. Channel Band-Width <= 80MHz (with 2MHz spacing)
viii. Frequency Hopping = Yes.
ix. Loop Filter reconfiguration= Required
x. Power Consumption < 2.5mWatt (25% of total Tx/Rx power)

6. I have gone through the Project Proposal submitted by Prof. P. Chandra Sekhar of Osmania University College of Engineering (A) for MeitY funding and noted the obligations and terms and conditions. I understand the responsibilities indicated in our name as stated below:

a) To provide commercially driven state of the art technical specification required for the project-A.
b) To provide necessary technical information, guidance, and support for the successful execution of the project.
c) To attend Project review meetings by nominating a suitable representative along with the representatives of the other parties involved in the execution of Project.
d) To release the funds promised for the execution of the project in appropriate time frame as specified in the proposal of project based on approved milestones.
e) To help characterize/test and validate the fabricated ASIC.
f) To obtain necessary certification for the final IP core.
g) To be responsible for industry level validation for the ASIC.
h) To commercialize the developed IPs.in the Project.

7. I hereby affirm that my Organization/Industry is committed to participate in the Project to the full extent as indicated in the Project Proposal. A summary profile of my organization is given below:

***BITSILICA** is supporting clients in developing complex ASICs/SoCs with our expertise in processors, mobile, networking, automotive, 5G and multimedia technologies. We offer a wide range of 'Concept-to-Pre-Silicon' Design services including Design Specification, RTL Design, Functional Verification, Logic Synthesis, Physical Design and STA. At present we offer services to more than 20 clients at various stages of SOC development.*

Rajasekharam Naidu P

Director Embedded Solutions,
BITSILICA Pvt. Ltd.

Date: 07/10/2022
Place: Hyderabad

BITSILICA PRIVATE LTD. HYDERABAD